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(54) Method of manufacturing low resistivity p-type compound semiconductor material

(57) The present invention provides a method of manufacturing a low resistivity p-type compound semiconductor material over a substrate. The method of the present invention comprises the steps of forming a p-type impurity doped compound semiconductor layer on the substrate by either HVPE, OMVPE or MBE and applying a microwave treatment over the p-type impurity doped compound semiconductor layer for a period of time. The high resistivity p-type impurity doped compound semiconductor layer is converted into a low resistivity p-type compound semiconductor material according to the present invention.

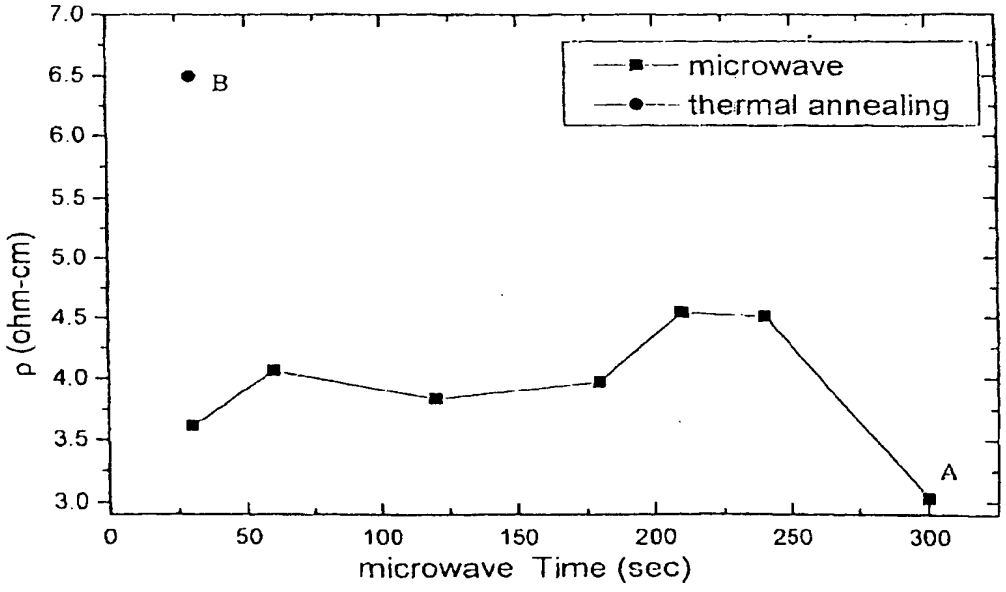

Fig. 2(a)

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D scription

BACKGROUND OF THE INVENTION

1. Field of the invention

[0001] The present invention relates to a method of manufacturing a compound semiconductor material, and more particularly, to a method of manufacturing a low resistivity p-type compound semiconductor material.

2. Description of the prior art

[0002] Most of the semiconductor devices such as light emitting diode, laser diode, photodetector, and transitior normally need some layers doped with n-type dopants and some layers doped with p-type dopants. However, some III-V and II-VI compound semiconductor materials are difficult to dope the p-type impurity in high carrier concentration, or even can't achieve p-type conductivity. For example, p-type InP, AlGaInP and AlGaInN III-V compound semiconductor materials and ZeSSe II-VI compound semiconductor materials are some typical examples that are either difficult to achieve high p-type conductivity or even impossible to get the p-type conductivity. One of the major reasons why it is difficult to achieve high carrier concentration in these p-type doping materials is attributed to the unintentional hydrogen incorporation and resulting acceptor passivation which occurs during the epitaxial growth or after the cool-down process of growth.

[0003] The influence of the cooling ambiance on the passivation of Zn acceptors in InP grown by atmospheric-pressure OMVPE was first studied by Antell et al. [Appl. Phys. Lett., 53, (1988), 758] and Cole et al. [Electron. Lett., 24, (1988), 929]. They found that the p-type InP layer capped with a p-type InGaAs and cooled down in an AsH_3 ambiance, the hole carrier concentration could be significantly reduced by about 80% compared to a Zn-doped InP layer with a n-type cap layer. The hole carrier concentration can be recovered to the expected value simply by annealing in nitrogen atmosphere.

[0004] The hydrogen passivation is even more serious in a p-type AlGaInP material, especially in a high aluminum content AlGaInP material. Hamada et al. [IEEE J. Quantum Electron. 27, (1991), 1483] found that the degree of passivation increased with aluminum composition. An increase in hole carrier concentration after annealing at 500 degree centigrade was observed and proved by a decrease in hydrogen content using SIMS analysis.

[0005] The hydrogen passivation effect is the most serious issue in AlGaInN materials. It causes the AlGaInN materials fail d to achieve p-typ conductivity. Akasaki et al. [Japanese J. Appl. Phys. 28, (1989), L2112] us d low energy electron b am irradiation (LEEBI) to convert the compensated Mg-doped GaN into conductive p-type material. However, with acceleration voltage of 5kV-15kV, an electron beam can only reach a depth of about 0.5μm. In device design, normally a p-type GaN material with a thickness of more than 0.5μm is necessary. Therefore, LEEBI is not an effective way to convert the thick high resistivity Mg-doped GaN material into p-type conducting material. Besides, the conversion of the p-type GaN material is achieved by scanning the electron beam across the whole wafer. This electron beam scanning method is a quite slow process. It is very difficult to be adapted into the mass production process by the electron beam scanning method.

[0006] In US patent No. 5,306,662, Nakamura et al. disclosed a method for reducing the resistivity of the p-type GaN by an annealing process in a nitrogen atmosphere over 400 degree centigrade approximately. But to be more effective, the annealing process should be carried out in the temperature range of 600-1200 degree centigrade. Therefore, it is not suitable for III-V compound semiconductor materials that have high dissociation pressure at low temperature without a protective cap layer.

SUMMARY OF THE INVENTION

[0007] It is therefore a primary objection of the present invention to provide a method of manufacturing a low resistivity p-type compound semiconductor material to solve the above mentioned problem.

[0008] According to the first aspect of the present invention, there is provided a method of manufacturing a low resistivity p-type compound semiconductor material over a substrate. The method of the present invention comprises the steps of:

> forming a p-type impurity doped III-V compound semiconductor layer on the substrate; and
> applying a microwave treatment over the p-type impurity doped III-V compound semiconductor layer.

[0009] According to the second aspect of the present invention, there is provided a method of manufacturing a low resistivity p-type compound semiconductor material over a substrate. The method of the present invention comprises the steps of:

> forming a p-type impurity doped II-VI compound semiconductor layer on the substrate; and
> applying a microwave treatment over the p-type impurity doped II-VI compound semiconductor layer.

[0010] According to the third aspect of the present invention, there is provided a method of manufacturing a light mitting diode. The light emitting diod comprises a substrate, a n-type lower cladding formed on the substrate, and an active layer formed on the n-type lower cladding layer. The method of the present invention comprises the steps of:

forming an p-type impurity doped upper cladding layer on the active layer; and
applying a microwave treatment over the p-type impurity doped upper cladding layer.

[0011] According to the fourth aspect of the present invention, there is provided a method of manufacturing a light emitting diode. The light emitting diode comprises a substrate. The method of the present invention comprises the steps of:

forming an p-type impurity doped lower cladding layer on the substrate;
applying a microwave treatment over the p-type impurity doped lower cladding layer;
forming an active layer on the p-type impurity doped lower cladding layer; and
forming a n- type upper layer on the active layer.

[0012] The present invention provides a simple and effective way to convert the high resistivity p-type impurity doped III-V or II-VI compound semiconductor materials into conductive p-type materials. According to the present invention, the p-type impurity doped III-V or II-VI compound semiconductor materials are grown by either hydride vapor phase epitaxy (HVPE), organometallic vapor phase epitaxy (OMVPE), or molecular beam epitaxy (MBE). The p-type impurity doped III-V or II-VI compound semiconductor materials normally have high resistivity due to hydrogen passivation effect. The high resistivity p-type impurity doped III-V or II-VI compound semiconductor materials are then treated in a microwave apparatus for a period of time in order to convert them into high conductive p-type materials.

[0013] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment which is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Fig. 1 is a schematic diagram of a test structure according to the present invention.

[0015] Fig. 2(a) is a resistivity versus activate time diagram of the Mg-doped GaN layer shown in Fig. 1.

[0016] Fig. 2 (b) is a carrier concentration versus activate time diagram of the Mg-doped GaN layer shown in Fig. 1.

[0017] Fig. 3 is a diagram showing the photoluminescence spectrum of the Mg doped GaN (a) without any treatment, (b) with the resistance furnace annealing, (c) with the microwave treatment.

[0018] Fig. 4 is a schematic diagram of a light emitting diode according to the present invention.

[0019] Fig. 5 is another schematic diagram of a light mitting diode according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0020] The present invention is to provide an easy and effective method of manufacturing a low resistivity p-type compound semiconductor material. According to the method of the present invention, first of all, a p-type impurity doped compound semiconductor layer is grown either directly or indirectly on a substrate by either HVPE, OMVPE or MBE. For III-V compound semiconductor material, the p-type impurity doped compound semiconductor layer can be an $Al_xGa_yIn_{1-x-y}P$ (where $0 \leq x \leq 1$, $0 \leq y \leq 1-x$) layer or an AlGaInN layer. The p-type dopant can be an element chosen from the group consisting of Zn, Cd, Be, Mg, Ca, and Ba. For II-VI compound semiconductor material, the p-type impurity doped compound semiconductor layer can be a ZnSSe layer. The p-type dopant can be an element chosen from the group consisting of Li, Na, K, N, P, and O. Due to the hydrogen passivation effect, the p-type impurity doped compound semiconductor layer will have a lower hole carrier concentration or even very high resistivity. Secondly, the substrate is pre-heated to a temperature that is below 400 degree centigrade to prevent the p-type impurity doped compound semiconductor layer cracking. The purpose of maintaining the substrate at a temperature above room temperature and below 400 degree centigrade is to pre-heat the substrate and to prevent the cracking of the substrate during the microwave treatment. Because the microwave treatment is a very low temperature process, it can be applied not only for $Al_xGa_yIn_{1-x-y}N$ (where $0 \leq x \leq 1$, $0 \leq y \leq 1-x$) material but also for InP, AlGaInP and ZnSe materials which have high dissociation pressure at low temperature. The preheating of the substrate can be preformed by a resistance heating process or an infrared lamp heating process. Besides, in the present invention, the p-type impurity doped compound semiconductor material also can be pre-heated at a temperature above 400 degree centigrade. Finally, the p-type impurity doped compound semiconductor layer is applied by a microwave treatment in a microwave apparatus which also has the resistance heating function. The p-type impurity doped compound semiconductor layer is then treated in a microwave apparatus for a period of time and converted into a low resistivity p-type compound semiconductor material.

[0021] The present invention will herein be described in detail with reference to the following embodiments and their accompanying drawing.

Embodiment 1

[0022] Please refer to Fig. 1. Fig. 1 is a schematic diagram of an as-grown sample 10 according to the present invention. An epitaxy-ready sapphire substrate 12 is loaded into the OMVPE reactor chamber (not shown). The sapphire substrate 12 is preheated for 10

min at 1150 degree c ntigrade. The temperature of the sapphire substrate 12 is then lowered to about 500-600 degree centigrade. At a t mperature of 520 degre centigrade, a 25nm thick GaN buffer layer 14 is grown on the sapphire substrate 12. The temperature is again raised to 1100 degree centigrade and a 4μm thick Mg-doped GaN layer 16 is grown on the buffer layer 14 with a growth rate about 2μm/hr.

[0023] Fig. 2(a) is a resistivity versus activate time diagram of the Mg-doped GaN layer 16 shown in Fig. 1. The as-grown sample 10 is then put into a microwave apparatus (not shown) which also has the resistance heating function. First, the as-grown sample 10 is pre-heated at a temperature about 60 degree centigrade to homogenize the temperature distribution across the whole wafer 10. After that, a 2.45GHz microwave with output power of 560W is applied to the Mg-doped GaN layer 16 for 5 min to activate the p-type dopants. The corresponding resistivity of the Mg-doped GaN layer 16 with microwave treatment is shown as the point A of the Fig. 2(a). For comparison, a Mg-doped GaN sample (not shown) with the same growth conditions is annealed at a temperature of 730 degree centigrade for 20 min and the corresponding resistivity of the furnace annealed Mg-doped GaN sample is shown as the point B of the Fig. 2 (a). The carrier concentration of the Mg-doped GaN layer 16 with microwave treatment is above $1\times10^{17}/cm^3$ by Hall measurement. The carrier concentration of the furnace annealed Mg-doped GaN sample is about $1\times10^{17}/cm^3$ and nearly smaller than the carrier concentration of Mg-doped GaN layer 16 with the microwave treatment, as comparing the point A and the point B shown in Fig. 2 (b). Furthermore, as shown in Fig. 2(a) and Fig. 2(b), around 30 seconds for the microwave treatment upon the Mg-doped GaN layer 16 can also show the good result of small resistivity and high carrier concentration.

[0024] Please refer to Fig. 3. Fig. 3 is a diagram showing the photoluminescence spectrum of a Mg-doped GaN 16 (a) without any treatment, (b) with the resistance furnace annealing, (c) with the microwave treatment. The Mg-doped GaN layer 16 with the microwave treatment and the Mg-doped GaN layer sample with resistance furnace annealing both shows a strong 4375 angstrom blue peak compared with the as-grown sample without any treatment. From both Hall measurement and photoluminescence spectrum, it proves that the microwave treatment is as effective as the resistance furnace annealing in converting the high resistivity material into the high conductive p-type material.

Embodiment 2

[0025] Please refer to Fig. 4. Fig. 4 is a schematic diagram of a light emitting diode 20 according to the present invention. The present invention is also to provide a method of manufacturing a light emitting diode 20 with a sapphire substrate 22. A GaN buffer layer 24 is grown on the sapphire substrate 22. The sapphire substrate 22 is then heated to about 1130 degree centigrade. A 4μm n-type Si-doped GaN layer 26 is grown on the buffer layer 24. The sapphire substrate 22 is then cooled down to about 820 degree centigrade. An InGaN/GaN multiple quantum well structure 28 is grown on the top of the n-type Si-doped GaN layer 26. Finally, a p-type Mg-doped GaN layer 30 is grown on the InGaN/GaN multiple quantum well structure 28 to form the light emitting diode 20. The light emitting diode 20 is then put into a microwave apparatus (not shown) that also has the resistance heating function. The light emitting diode 20 is pre-heated at a temperature of about 60 degree centigrade. After that, a 2.45GHz microwave with output power of 560W is applied to the light emitting diode 20 for 3 min to activate the p-type dopants.

[0026] Besides, the light emitting diode 20 with the microwave treatment is then processed into LED chips according to the following steps.

(1) The surface of the p-type GaN layer 30 is partially etched until the n-type GaN layer 26 is exposed.
(2) A Ni/Au ohmic contact metal 32 is evaporated onto the p-type GaN layer 30 and a Ti/A1 ohmic contact metal 34 is deposited onto the n-type GaN layer 26.
(3) The metallized light emitting diode 20 is then scribed and broken into a square shape chip with a size of 350μm×350μm.

Finally, the LED chip fabricated as described above has a forward voltage about 3.5 volt and this forward voltage value is similar to the LED chips made with the furnace annealing.

Embodiment 3

[0027] Please refer to Fig. 5. Fig. 5 is another schematic diagram of a light emitting diode 40 according to the present invention. The present invention is also to provide a method of manufacturing a light emitting diode 40 with a sapphire substrate 42. A GaN buffer layer 44 is grown on the sapphire substrate 42. The sapphire substrate 42 is then heated to about 1120 degree centigrade. A 4μm p-type Mg-doped GaN layer 50 is grown on the buffer layer 44. The p-type Mg-doped GaN layer 50 is then put into a microwave apparatus (not shown) that also has the resistance heating function. The sapphire substrate 42 is pre-heated at a temperature of about 60 degree centigrade. After that, a 2.45GHz microwave with output power of 560W is applied to the p-type Mg-doped GaN layer 50 for 3 min to activate the p-type dopants. And then, the sapphire substrate 42 is then cooled down to about 820 degree c ntigrade. An INGaN/GaN multiple quantum well structure 48 is grown on the top of the p-typ Mg-doped GaN layer 50. Th sapphire substrate 42 is then heated to about 1130 de-

gree centigrade. A n-type Si-doped GaN layer 46 is grown on the InGaN/GaN multiple quantum well structure 48 to form the light emitting diode 40.

[0028] Besides, the light emitting diode 40 with the microwave treatment is then processed into LED chips according to the following steps.

(1) The surface of the n-type GaN layer 46 is partially etched until the p-type GaN layer 50 is exposed.
(2) A Ni/Au ohmic contact metal 52 is evaporated onto the p-type GaN layer 50 and a Ti/Al ohmic contact metal 54 is deposited onto the n-type GaN layer 46.
(3) The metallized light emitting diode 40 is then scribed and broken into a square shape chip with a size of 350μm×350μm.

Finally, the LED chip fabricated as described above has a forward voltage about 3.5 volt and this forward voltage value is similar to the LED chips made with the furnace annealing.

Embodiment 4

[0029] The present invention is also to provide a method of manufacturing a light emitting diode 40 with a sapphire substrate 42. A GaN buffer layer 44 is grown on the sapphire substrate 42. The sapphire substrate 42 is then heated to about 1120 degree centigrade. A 4μm p-type Mg-doped GaN layer 50 is grown on the buffer layer 44. And then, the sapphire substrate 42 is then cooled down to about 820 degree centigrade. An INGaN/GaN multiple quantum well structure 48 is grown on the top of the p-type Mg-doped GaN layer 50. The sapphire substrate 42 is then heated to about 1130 degree centigrade. A n-type Si-doped GaN layer 46 is grown on the InGaN/GaN multiple quantum well structure 48 to form the light emitting diode 40. The p-type Mg-doped GaN layer 50 is then put into a microwave apparatus (not shown) that also has the resistance heating function. The sapphire substrate 42 is pre-heated at a temperature of about 60 degree centigrade. After that, a 2.45GHz microwave with output power of 560W is applied to the p-type Mg-doped GaN layer 50 for 3 min to activate the p-type dopants.

[0030] Besides, the light emitting diode 40 with the microwave treatment is then processed into LED chips according to the following steps.

(1) The surface of the n-type GaN layer 46 is partially etched until the p-type GaN layer 50 is exposed.
(2) A Ni/Au ohmic contact metal 52 is evaporated onto the p-type GaN layer 50 and a Ti/Al ohmic contact metal 54 is deposited onto the n-type GaN layer 46.
(3) The metallized light emitting diode 40 is then scribed and broken into a square shape chip with a size of 350μm×350μm.
Finally, the LED chip fabricated as described above has a forward voltage about 3.5 volt and this forward voltage value is similar to the LED chips made with the furnace annealing.

[0031] With the example and explanations above, the features and spirits of the invention will be hopefully well described. Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Claims

1. A method of manufacturing a low resistivity p-type compound semiconductor material over a substrate, the method comprising the steps of:

   (a) forming a p-type impurity doped compound semiconductor layer on the substrate; and
   (b) applying a microwave treatment over the p-type impurity doped compound semiconductor layer.

2. The method of the claim 1 wherein the p-type impurity doped compound semiconductor layer is an $Al_xGa_yIn_{1-x-y}P$ layer, and $0_{\leq x\leq 1, 0\leq y\leq 1-x}$.

3. The method of claim 1 wherein the p-type impurity doped compound semiconductor layer is an $Al_xGa_yIn_{1-x-y}N$ layer, and $0_{\leq x\leq 1, 0\leq y\leq 1-x}$

4. The method of claim 1 wherein the p-type impurity doped compound semiconductor layer is a ZnSSe layer.

5. The method of claim 2 wherein the p-type impurity is at least one selected from the group consisting of Zn, Cd, Be, Mg, Ca, and Ba.

6. The method of claim 3 wherein the p-type impurity is at least one selected from the group consisting of Zn, Cd, Be, Mg, Ca, and Ba.

7. The method of claim 4 wherein the p-type impurity is at least one selected from the group consisting of Li, Na, K, N, P, and O.

8. A method of manufacturing a light emitting diode, the light emitting diode comprising a substrate, a lower cladding layer of a first conductivity type formed on the substrat , and an active layer formed on the lower cladding layer, the method comprising

the steps of:

(a) forming an upper cladding layer of a second conductivity type on the active layer; and
(b) applying a microwav treatment over the upper cladding layer.

9. The method of the claim 8 wherein the upper cladding layer is an $Al_xGa_yIn_{1-x-y}P$ layer, and $0_{\leq x \leq 1,\ 0 \leq y \leq 1-x}$.

10. The method of claim 8 wherein the upper cladding layer is an $Al_xGa_yIn_{1-x-y}N$ layer, and $0_{\leq x \leq 1}$, $0_{\leq y \leq 1-x}$.

11. The method of claim 8 wherein the upper cladding layer is a ZnSSe layer.

12. The method of claim 9 wherein the upper cladding layer is doped by at least one selected from the group consisting of Zn, Cd, Be, Mg, Ca, and Ba.

13. The method of claim 10 wherein the upper cladding layer is doped by at least one selected from the group consisting of Zn, Cd, Be, Mg, Ca, and Ba.

14. The method of claim 11 wherein the upper cladding layer is doped by at least one selected from the group consisting of Li, Na, K, N, P, and O.

15. A method of manufacturing a light emitting diode, the light emitting diode comprising a substrate, the method comprising the steps of:

(a) forming a lower cladding layer of a first conductivity type on the substrate;
(b) applying a microwave treatment over the lower cladding layer;
(c) forming an active layer on the lower cladding layer of the first conductivity type; and
(d) forming an upper layer of a second conductivity type on the active layer.

16. A method of manufacturing a light emitting diode, the light emitting diode comprising a substrate, the method comprising the steps of:

(a) forming a lower cladding layer of a first conductivity type on the substrate;
(b) forming an active layer on the lower cladding layer of the first conductivity type; and
(c) forming an upper layer of a second conductivity type on the active layer;
(d) applying a microwave treatment over the lower cladding layer.

17. Th method of the claim 15 or 16 wherein the lower cladding layer is an $Al_xGa_yIn_{1-x-y}P$ layer, and $0_{\leq x \leq 1}$, $0_{\leq y \leq 1-x}$.

18. The method of claim 15 or 16 wher in the lower cladding layer is an $Al_xGa_yIn_{1-x-y}N$ layer, and $0_{\leq x \leq 1,\ 0 \leq y \leq 1-x}$.

19. The method of claim 15 or 16 wherein the lower cladding layer is a ZnSSe layer.

20. The method of claim 17 wherein the lower cladding layer is doped by at least one selected from the group consisting of Zn, Cd, Be, Mg, Ca, and Ba.

21. The method of claim 18 wherein the lower cladding layer is doped by at least one selected from the group consisting of Zn, Cd, Be, Mg, Ca, and Ba.

22. The method of claim 19 wherein the lower cladding layer is doped by at least one selected from the group consisting of Li, Na, K, N, P, and O.

23. The method of claim 8 wherein the first conductivity type is a n-type, and the second conductivity type is a p-type.

24. The method of claim 15 or 16 wherein the first conductivity type is a p-type, and the second conductivity type is a n-type.

25. The method of one of the claims 1, 23 or 24 wherein the method further comprises, between the step (a) and step (b), a step (e) of pre-heating the substrate at a predetermined range of temperature.

26. The method of the claim 25 wherein the predetermined range of temperature is below 400 degree centigrade.

27. The method of the claim 26 wherein the step (e) is performed by a resistance heating process.

28. The method of the claim 27 wherein the step (e) is performed by an infrared lamp heating process.

29. The method of one of the claims 1, 8, 15 or 16 wherein the step (a) is performed by a hydride vapor phase epitaxy process.

30. The method of one of the claims 1, 8, 15 or 16 wherein the step (a) is performed by an organometallic vapor phase epitaxy process.

31. The method of one of the claims 1, 8, 15 or 16 wherein the step (a) is performed by a molecular beam epitaxy process.

32. The method of one of the claims 1, 8, 15 or 16 wherein the substrate is an epitaxy-ready sapphire substrate.

33. The method of one of the claims 1, 8, 15 or 16 wherein the step (b) is performed by a 2.45GHz microwave with output power of 560W.

34. The method of one of the claims 8, 15 or 16 wherein the active layer is a multiple quantum well structure.

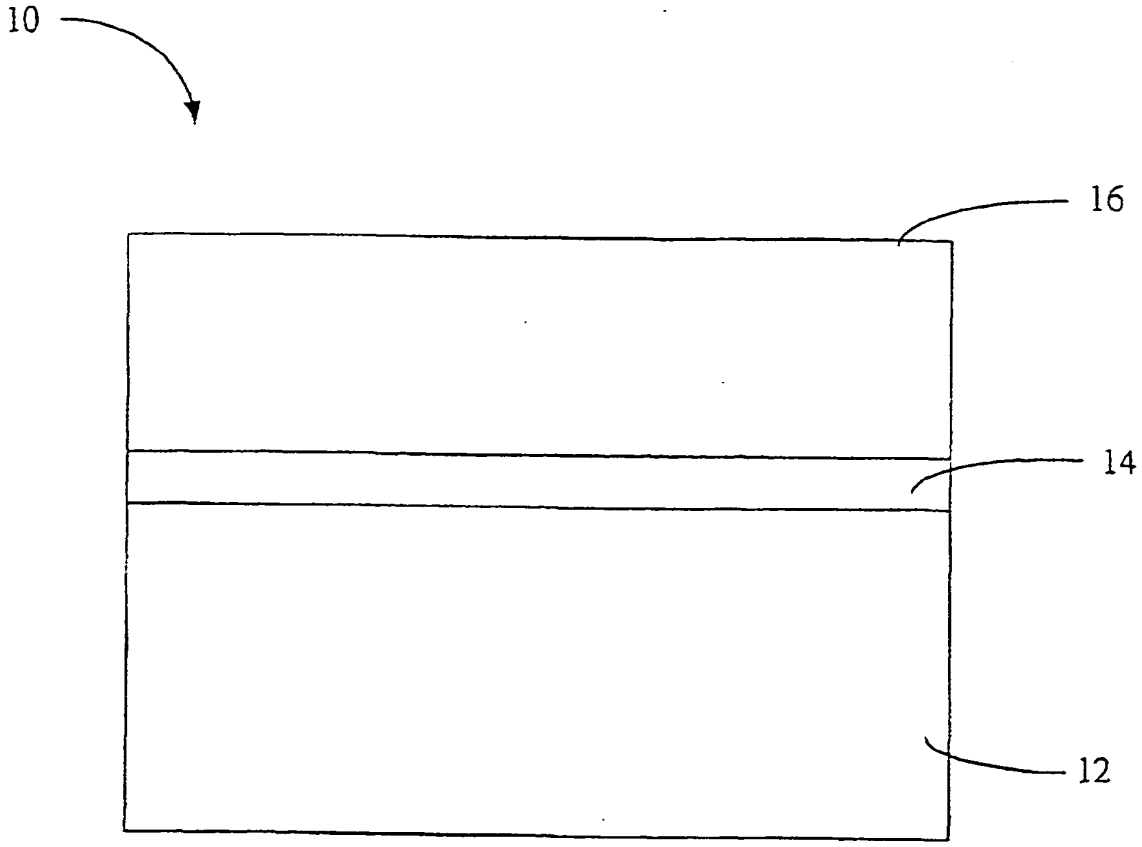

Fig. 1

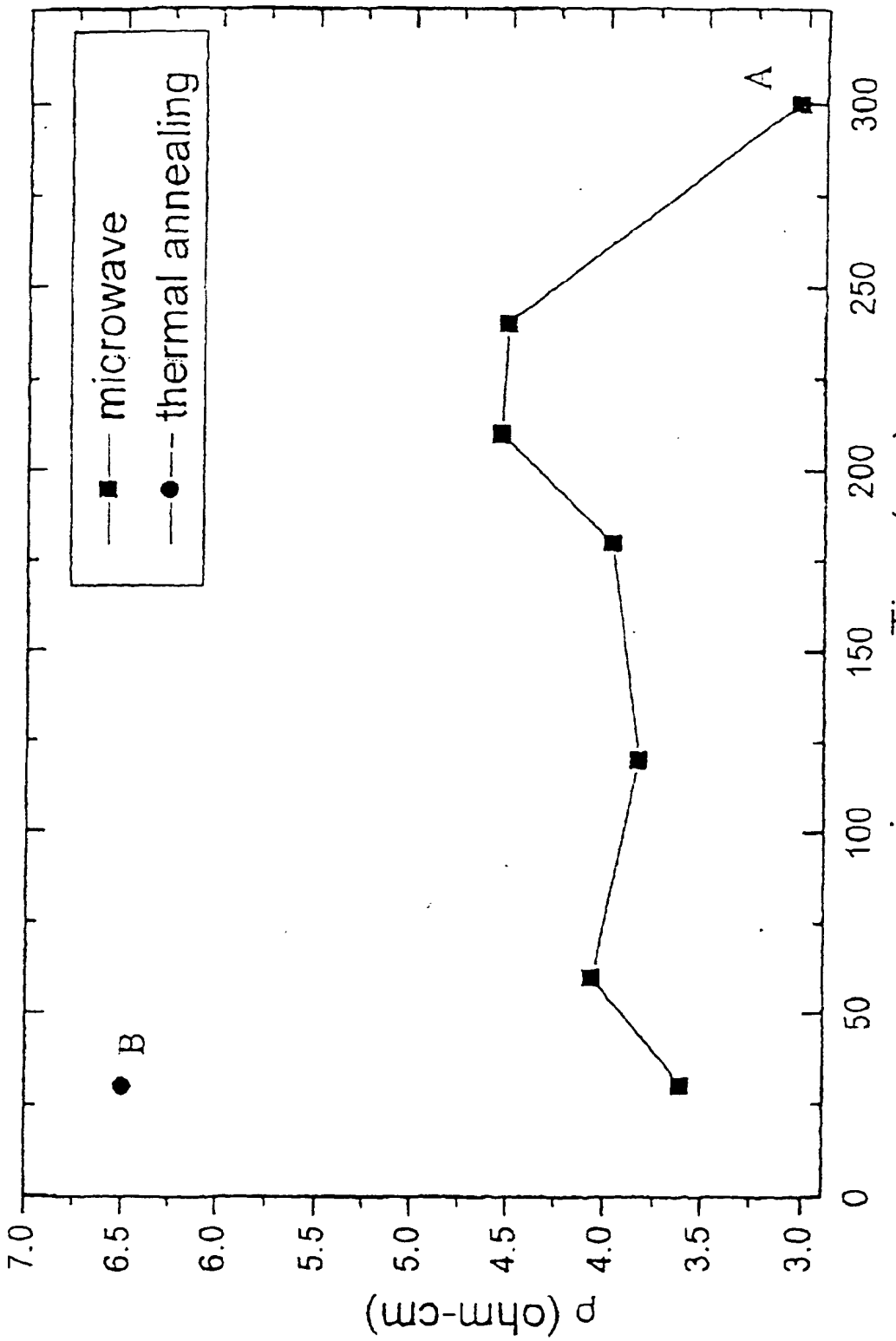

Fig. 2(a)

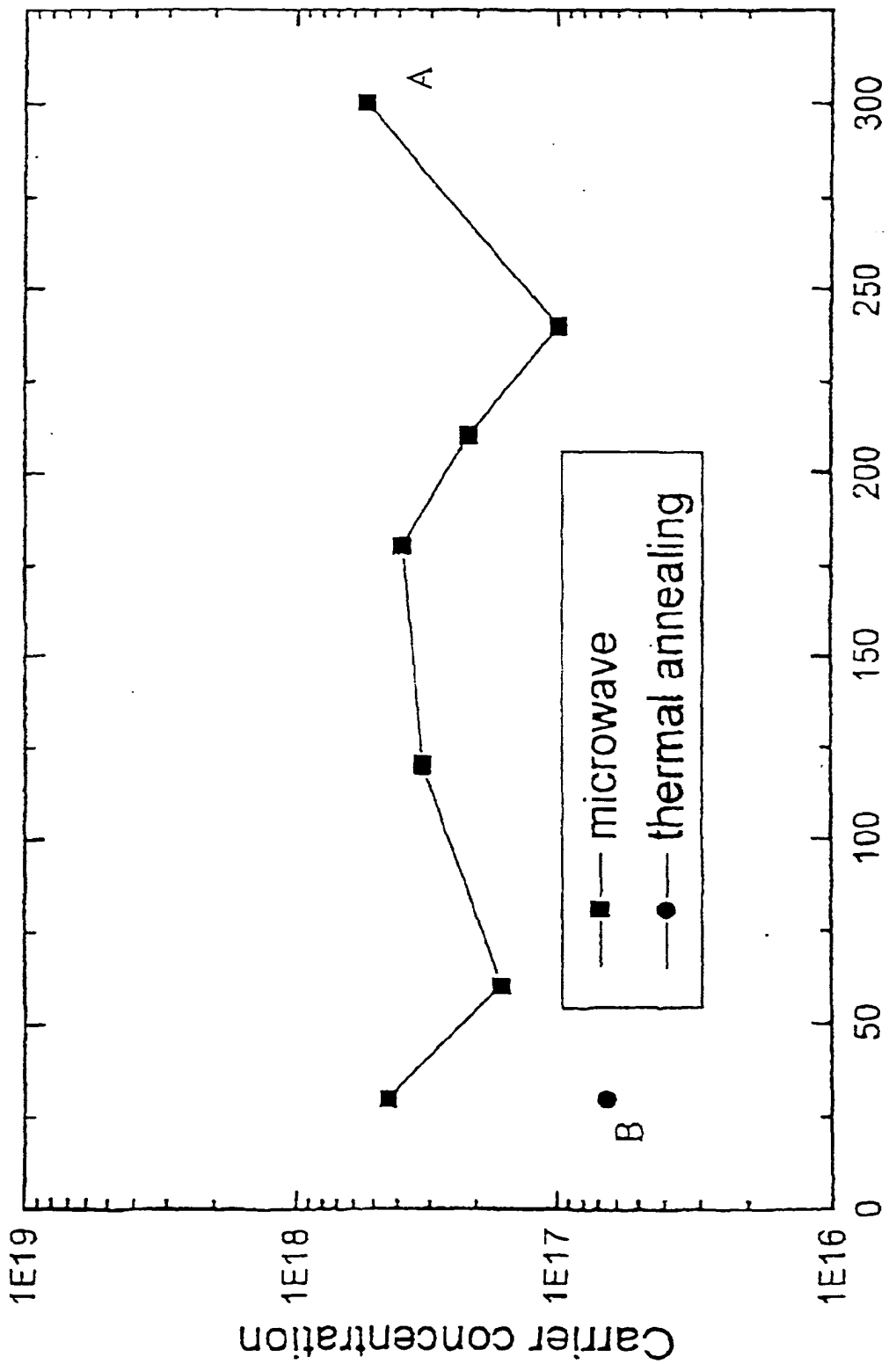

Fig. 2(b)

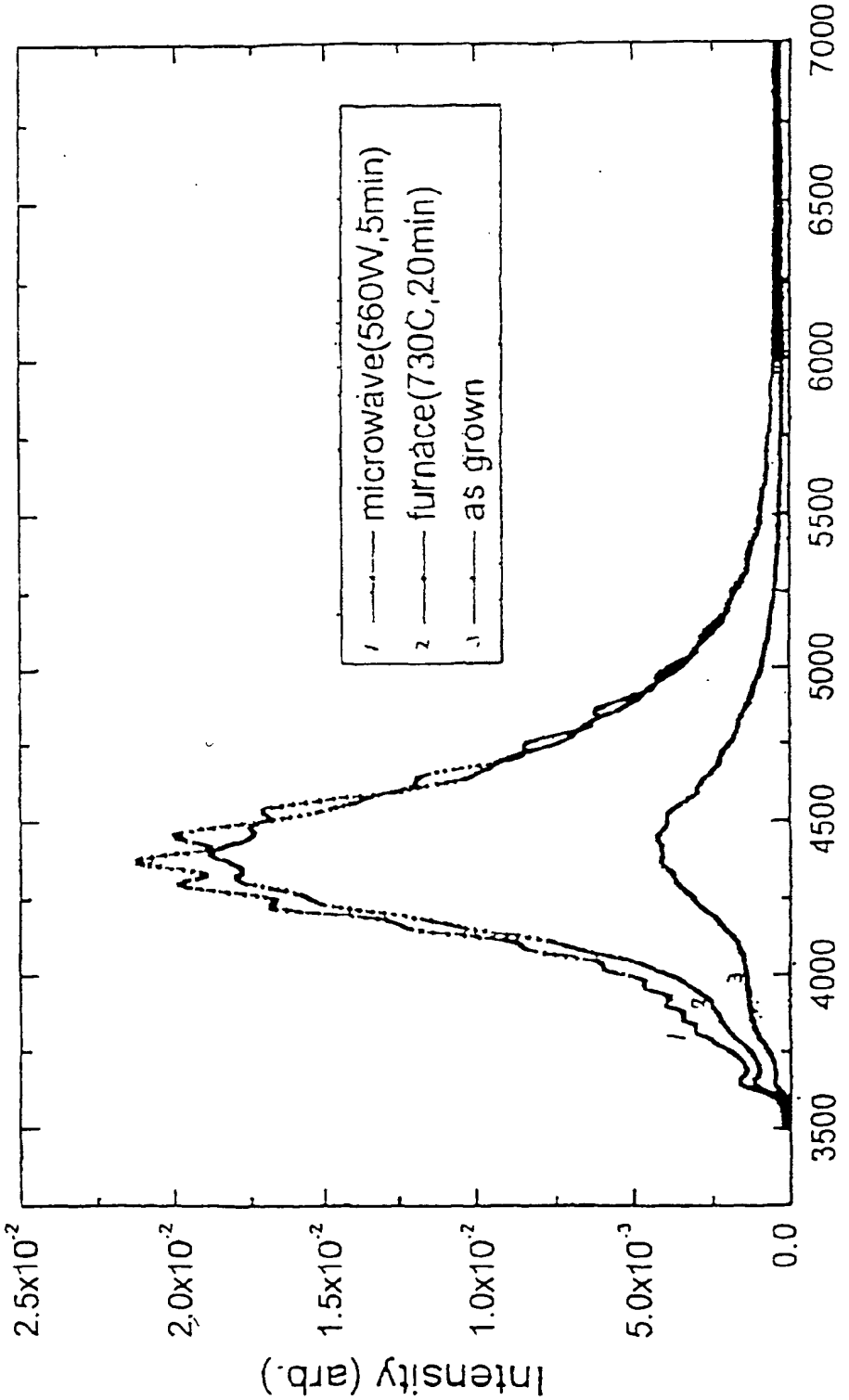

Fig. 3

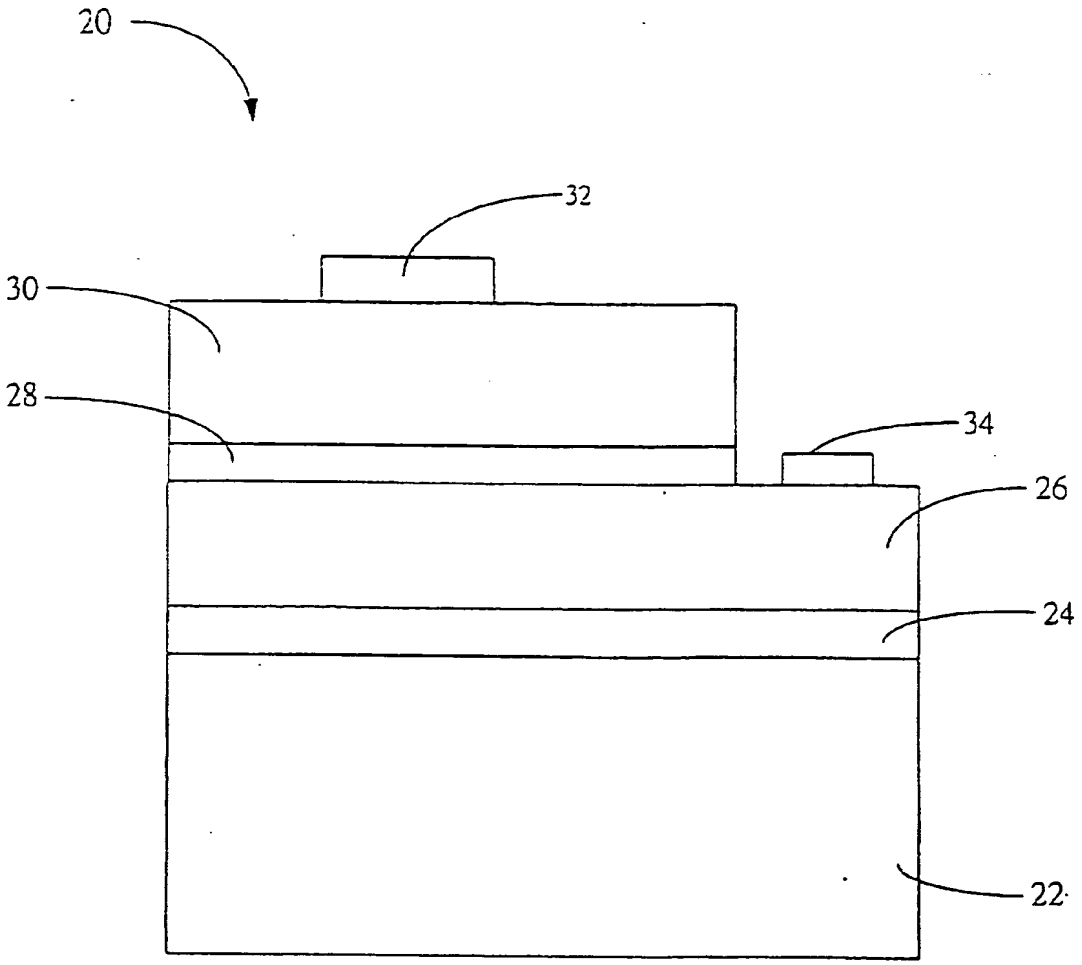

Fig. 4

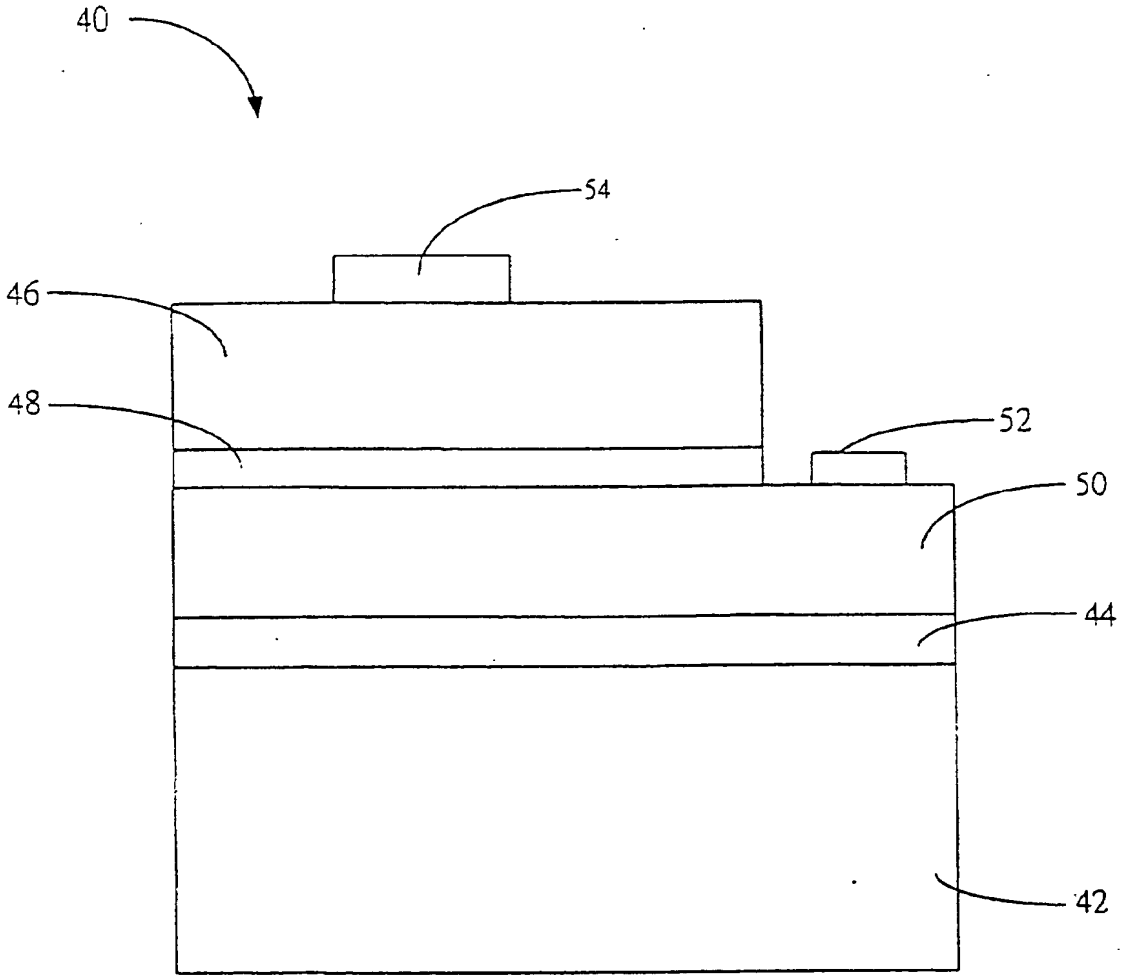

Fig. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 10 4723

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	PEARTON S J: "ION BEAM PROCESSING AND RAPID THERMAL ANNEALING OF INP AND RELATED COMPOUNDS" PROCEEDINGS OF THE INDIUM PHOSPHIDE AND RELATED MATERIALS CONFERENCE,US,NEW YORK, IEEE, vol. CONF. 2, 1990, pages 379-388, XP000170255	1	H01L33/00 H01L21/268 H01L21/324 H01L21/428
Y	* the whole document *	2-34	
D,Y	US 5 306 662 A (NAKAMURA SHUJI ET AL) 26 April 1994 (1994-04-26) * column 1-12 *	1-34	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	5 June 2000	Wolff, G

CATEGORY OF CITED DOCUMENTS

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05-06-2000

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